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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,985	03/08/2002	Steven H. Voldman	BUR920020014	2597
24241	7590	12/20/2005	EXAMINER	
IBM MICROELECTRONICS INTELLECTUAL PROPERTY LAW 1000 RIVER STREET 972 E ESSEX JUNCTION, VT 05452			NADAV, ORI	
		ART UNIT	PAPER NUMBER	2811
DATE MAILED: 12/20/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/683,985	VOLDMAN, STEVEN H.
	Examiner Ori Nadav	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 September 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 26-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 26-42 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some *
 - c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION***Claim Objections***

Claims 26-42 are objected to because of the following informalities: The phrase "without removing any portion of said original substrate and replacing with another substrate material" should read "without removing any portion of said original substrate and without replacing with another substrate material". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26, 28, 35, 37-39 and 41-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Beasom (5,841,169).

Beasom teaches in figure 2 and related text a method of forming a diode on an original substrate, comprising the steps of forming an anode 202 of a first conductivity type and a cathode 204 of a second conductivity type disposed below said anode on said original substrate 201 without removing any portion of said original substrate and replacing with another substrate material, wherein at least one of said cathode and anode comprise a plurality 207, 202 of vertically abutting diffusion regions; and etching said substrate (column 4, lines 14-53) to form a plurality of isolation regions 209, 219 in said original

substrate, said cathode and anode being disposed between adjacent ones of said plurality of isolation regions, said plurality of isolation regions extending deeper into said original substrate than said cathode and said anode.

Regarding claim 28, Beasom teaches in figure 2 and related text isolation regions comprise a plurality of insulation-filled trenches having sidewalls that are tapered.

Regarding claim 35, Beasom teaches in figure 2 and related text the step of forming said anode comprises the steps of:

forming a first doped region 202 abutting said cathode; and
forming a second doped region 207 on a surface of said substrate, said second doped region having a higher concentration of dopant than said first doped region.

Regarding claim 37, Beasom teaches in figure 2 and related text the steps of forming a plurality of diffusion regions 214, 215 of said second conductivity type on a surface of said substrate.

Regarding claim 38, Beasom teaches in figure 2 and related text the step of forming a plurality of second isolation regions 209, 219 that separate said plurality of diffusion regions from said cathode.

Regarding claims 39 and 41-42, Beasom teaches in figure 2 and related text said cathode being in electrical contact with said substrate, wherein a junction formed between said anode and said cathode is bounded by said adjacent ones of said plurality of isolation regions, and wherein said substrate comprises a single crystal material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 29 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beasom.

Regarding claim 29, Beasom teaches in figure 2 and related text teaches substantially the entire claimed structure, as applied to claim 26 above, except the step of forming a second doped region of said second conductivity type disposed below said first doped region and contacting said substrate, wherein said first and second doped regions having different dopant concentrations.

Beasom teaches in figure 4 and related text the step of forming a cathode comprises forming a first doped region 403 of a second conductivity type abutting said anode 402; and forming a second doped region 404 of said second conductivity type abutting and disposed below said first doped region and contacting said substrate 401, said first and

second doped regions having different dopant concentrations. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the step of forming said cathode comprises forming a first doped region 204 of a second doped region of said second conductivity type abutting and disposed below said first doped region and contacting said substrate, wherein said first and second doped regions having different dopant concentrations in Beasom's device in order to minimize the isolation leakage of the device.

Although Beasom does not explicitly state that layers 407, 402, 403 and 404 form a diode, layers 407, 402, 403 and 404 form a PN junction, and thus forming a diode.

Regarding claims 31 and 32, Beasom teaches in figure 2 and related text isolation regions are formed by a process comprising the steps of etching said substrate to form trenches and depositing at least one insulator and a fill material. Beasom does not teach removing portions of said insulator outside of said trenches. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to remove portions of said insulator outside of said trenches in order to form the device as depicted in figure 2 of Beasom.

Regarding claim 33, Beasom teaches in figure 2 and related text the step of forming said cathode further comprises the step of forming a third doped region 206 disposed between said first doped region and said second doped region.

Claims 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beasom in view of Mack et al. (4,736,271).

Regarding claim 27, Beasom teaches in figure 2 and related text teaches substantially the entire claimed structure, as applied to claim 26 above, except a plurality of insulation-filled trenches having sidewalls that are substantially vertical.

Mack et al. Teach in figure 11, a plurality of insulation-filled structures having sidewalls that are substantially vertical. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of insulation-filled trenches of Beasom's device with sidewalls that are substantially vertical in order to simplify the processing steps of making the device.

Regarding claim 30, Beasom teaches in figure 2 and related text teaches substantially the entire claimed structure, as applied to claims 26 and 29 above, except forming a second pair of isolation structures between said adjacent isolation regions and said anode.

Mack et al. teach in figure 11 forming a second pair of isolation structures 30 between said adjacent isolation regions 30 and anode 54, 60. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a second pair of isolation structures between said adjacent isolation regions and said anode in Beasom's device in order to provide better electrical isolation for the anode.

Claims 34, 36 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beasom in view of Robinson et al. (5,268,316).

Beasom teaches in figure 2 and related text teaches substantially the entire claimed structure, as applied to claims 26, 33 and 35 above, except a third doped region comprises a retrograde-doped region. Robinson et al. teach a third doped region comprises a retrograde-doped region (column 3, lines 36-47). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third doped region comprises a retrograde-doped region in Beasom's device in order to provide low-reverse leakage, a relatively low voltage turn-on, and low series resistance for the current path from the junction to the diode contact.

Regarding claim 40, Robinson et al. teach in figure 8 and related text a cathode is disposed entirely below an anode 6. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the cathode entirely below the anode in Beasom's device in order to improve the characteristics of the device.

Response to Arguments

Applicant argues that Beasom does not form an anode and a cathode on an original substrate without removing any portion of said original substrate and without replacing with another substrate material, because Beasom removes an entire portion

of the single crystal substrate where the diode regions are subsequently formed and fills the region with polysilicon.

Beasom teaches in figure 2 and related text forming an anode 202 of a first conductivity type and a cathode 204 of a second conductivity type on an original substrate 201, which is located below regions 208. No part of that original substrate 201 is neither removed nor replaced. Therefore, Beasom teaches forming an anode and a cathode on a substrate without removing any portion of said original substrate and without replacing with another substrate material, as claimed.

Note that forming an anode and a cathode on an original substrate without removing any portion of said original substrate and without replacing with another substrate material, as recited in claim 26, is not synonymous to the examiner's suggestion of reciting a claim limitation such as: providing an original substrate, not heavily doped with anode and cathode regions, and then doping said original substrate to form anode and cathode regions without removing and without replacing any portion of said original substrate.

Applicant argues that Beasom does not form a plurality of isolation regions in said original substrate, because Beasom removes an entire portion of the single crystal substrate.

The plurality of isolation regions are formed in the portion of the single crystal substrate which is removed from the original substrate. Therefore, Beasom teaches plurality of isolation regions formed in said original substrate, as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
12/15/05

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